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Case study of Mixed Signal Design Flow

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Abstract: *With the continuously expanding of market for portable devices such as wireless communication devices, portable computers, consumer electronics and implantable medical devices, low power is becoming increasingly important in integrated circuits. Also Mixed-signal designs are becoming more and more complex every day. In order to adapt to the new market requirements, a formal process for design and verification of mixed signal systems i.e. top-down design and bottom-up verification methodology is required. This methodology has already been established for digital design. The goal of this research is to propose a new design methodology for mixed signal systems. The proposed design flow is based on behavioral modeling of the mixed signal system using one of the mixed signal behavioral modeling languages. These models can be used for design and verification through different steps of the design from system level modeling to final physical design. The other advantage of the proposed flow is analog and digital co-design.*

I. Importance of design methodology in market share.

With the internet, security, automobile and wireless technology as the latest market drivers, the pace of the electronic market place continues to quicken. New products and new product categories are being created faster than ever before. In order to keep up with the rapid pace of the market, designers must get their products to market more quickly than ever. Those that are successful at bringing significant new capabilities to the market first are usually rewarded with higher profit margins and greater market share. To understand this, consider three scenarios for developing a product with Figure 1.1 showing the expected revenue for each scenario [1]. For the first, consider employing an efficient product development process and being first to market. For the second, consider using the same number of developers with an inefficient development process, which causes the product to be late to market.

This results in a much lower return because the product enters a market where a competitor has already established leader-ship position and because there are fewer available customers left. Finally, consider using an inefficient development process but increasing the number of developers in order to reach the market first. If this were possible, the development costs are higher, but the total return is almost the same as in the first case. This is because the returns are expected to be much greater than the initial development cost

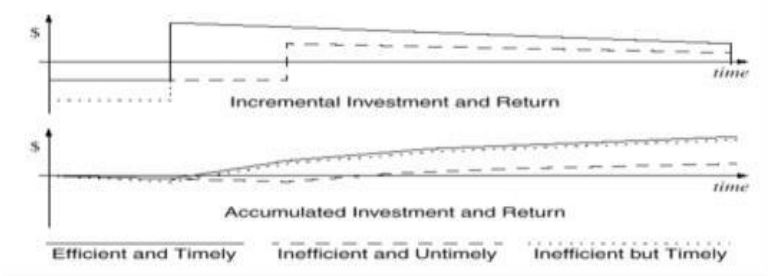

Figure: 1.1 Different approaches to design

This example illustrates why it is more important to get a product to the market first than it is to control development costs. Here, the market leadership position is largely determined and the need to develop the product in a timely manner is balanced by the need to control development costs. Moore's observation that the number of transistors available on an integrated circuit doubles every 18 to 24 months continues to hold. Competitive pressures compel designers to use these transistors to provide additional functionality and to increase the integration level and thereby decreasing the size, weight, power and cost of the prod-

The increasing size and complexity of these designs com- bines with the shrinking time available to develop and get them to market; making the job of the circuit designer today much more difficult than in the past Circuits are getting more complex in two different ways at the same time. First, circuits are becoming larger. Consider wireless products; 60 years ago a typical receiver contained between 5 and 10 transistors whereas it is common for a modern cell phone to contain 10M transistors. Second, the operation of the circuits

is becoming more complex.40 years ago integrated circuits generally consisted of simple functional blocks such as op-amps and gates. Verification typically required simulating the block for two or three cycles. Today, mixed-signal chips implement complex algorithms that require designers to examine their operation over thousands of cycles. Examples include PLLs (Phase Locked Loop), sigma-delta converters and CDMA (Code Division Multiple Access) transceivers.

The Computer Aided Design (CAD) tools and computers employed by designers continually improve, which serves to increase the productivity and accuracy of designers. The growing difference between the improvement in productivity needed to satisfy the demands of the market and the productivity available simply by using the latest CAD tools and computers is referred to as the Design Productivity Gap, and is shown in Figure 1.2 . To close this gap, one must change the way design is done. A design style that reduces the number of serial steps, increases the likelihood of first time working silicon, and increases the number of designers that can work together effectively is needed. If a design group fails to move to such a design style, it will become increasingly ineffective.

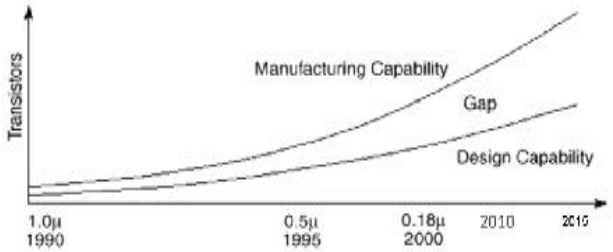

Figure:1.2 IC process technologies is improving faster than IC

II. Design Technology

1.1Bottom-up design.

In this approach the design process starts with the design of the individual blocks, which are then combined to form the system. The design of the blocks starts with a set of specifications and ends with a transistor level implementation. At this point, each block is verified as a stand-alone unit against specifications and not in the context of the over- all system. Once verified individually, the blocks are then combined and verified together. At this point the entire system is represented at the transistor level. While bottom-up design continues to be effective for small designs, large designs create several important problems with this approach.

*Once the blocks are combined, simulation takes a long time so verification becomes difficult and perhaps impossible. The amount of verification must be reduced to meet time-to-market goals .

*Any errors or problems found when assembling the system are expensive to fix because they involve redesign of the transistor-level blocks.

*Communication between designers is critical, yet an informal and error-prone approach to communication is usually employed.

On the other hand, generating digital signals in an analog simulation environment is difficult and in most of the cases the designer assumes simplified equivalent control signals. In this approach, the simulation of the overall system is only possible at the final stage of design and after completing the layout. Any changes at this stage are difficult and time consuming. Before the post-layout simulations, designers can only simulate the effect of digital and analog interactions at the system level.

By comparing different abstraction levels in the digital and analog design flows, we can see some similarities between the two flows. The second approach for designing the mixed signal system is based on analog-digital co-design. In this approach, after the system level design, the behavioral / RTL model of the overall system will be developed and verified. VHDL-AMS can be used to have a mixed signal model of the chip. The digital part would be described using a RTL synthesizable subset of the language, while the analog part would be partitioned into functional blocks at the functional or behavioral level, e.g. Filters, VCOs, op amps, etc. The whole model can be simulated using test benches written in VHDL-AMS. The next step is the block design which has different steps for digital and analog blocks. The digital part of the chip can be synthesized using a logic synthesizer to produce a gate level net list. Analog blocks are individually designed at the transistor level. After completing each block, it is possible to test the block in the interaction with other blocks using the test benches developed earlier. Standard cells place and route tools can produce the layout of the digital part from the gate level net list. The layout of the analog block is usually created manually or through dedicated module generators. From the layout the parasitic elements are extracted. Those elements related to the digital part are used to compute delays that are stored in SDF (Standard Delay Format) files. The final simulation can be done using the extracted layout view of the overall chip.

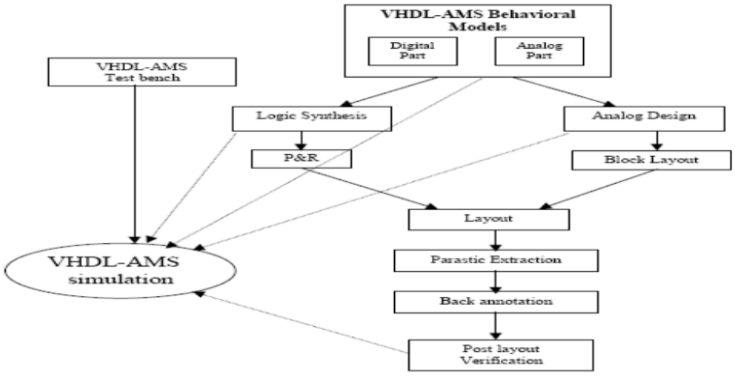

Figure: 2.2 Digital/Analog co design

III. Proposed mixed signal design flow

The proposed mixed signal design flow is based on analog- digital co-design methodology and has two distinguished levels of abstractions.

1 System Level Design, 2.Block Level Design

3.1System level Design

Set Design Goals: A design process starts with a clear statement of the problem, a search of existing state of the art solutions, clear objectives of the current design, and identification of a possible solution for achieving the objectives and selection of implementation for the solution. A marketing or preview spec can be generated at this point on paper for peer review. The specs should include descriptions of functions, estimated performance metrics (speed, power, noise, etc.) and projected operating constraints (bias, thermal, I/O impedance, proximity, etc.).

Preview Spec Gate: With goals and priorities set and re- sources planned, a peer review should be done to ensure that the overall scope of the design project is acceptable and the right decisions have been made before proceeding further.

System Level modeling: The preview system specs are captured with Matlab/Simulink or VHDL-AMS for a more precise definition and verification of the specs and to allow the exploration of appropriate architectures by using available modules from existing libraries and/or mathematical representations created by the designer. At this stage the use of re-usable (IP) blocks should be considered as their availability can have a strong impact on the selection of architecture and development time.

Packaging Selection: The designer should select the packaging solution early because the design or the final product will eventually need to interact with the outside world through its packaging and the packaging chosen may significantly affect the design's behavior. Considering Packaging effects in the early design stage is crucial. The decision on the packaging can have a strong impact on design. It can constrain partitioning, improve the accuracy of behavioral modeling if a packaging model is available and enhance the validity of simulation/ test plans.

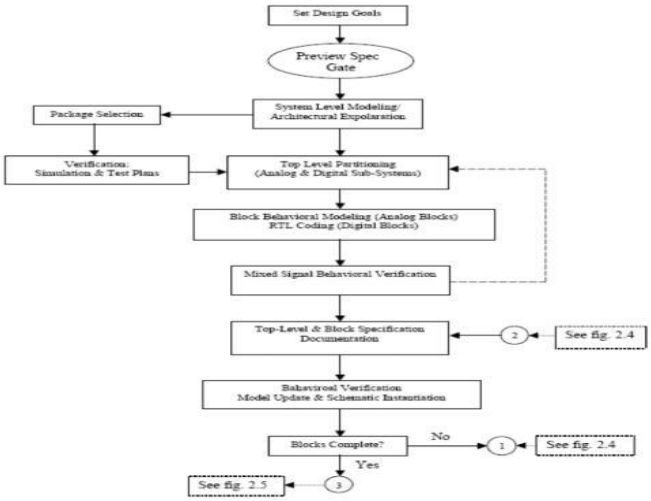

Figure: 2.3 System level

Verification: Simulation and Test Plan: In parallel to the architecture exploration, the verification strategy including simulation plan and test plan should be considered. The issues to be considered include how top level net list and each block or sub-block will be modeled and simulated, what types of simulations (transient, ac, noise, frequency domain) of simulations at each level will be used, how the stimuli will be created, how the interference between the blocks will be modeled, what tests to be performed, what test equipment to be used, how to bias the chip, what supply decoupling is satisfactory, what DFT techniques should be used to facilitate testing and diagnosis. Some of verification plan details can also be derived after design partitioning and behavioral modeling. It is an iterative process between verification planning and partitioning and behavioral modeling.

Top Level Partitioning: The architecture is partitioned into digital and analog blocks and each of the digital and analog blocks are further partitioned into basic sub blocks. The architecture must be partitioned in a way that maintains as much hierarchy as possible, makes use of common implementable functional blocks, minimize critical connections between blocks and must be consistent with the chosen packaging technology in terms of electrical, mechanical and thermal characteristics.

Block Behavioral and RTL coding : Behavioral modeling can be done for both analog and digital blocks using VHDL- AMS .The overall behavioral model of the system can be simulated and verified. There could be different levels of abstraction for each behavioral model starting with

Gate Level Simulation: The gate level simulation enables the designer to check the functionality of the structural net list against the RTL simulation. The test bench used previously for the RTL simulation is used here. Using VHDL-AMS, the de- signer can verify the functionality of the synthesized block in interaction with analog blocks.

Floor planning: This steps involves the creation of rows around the perimeter of the design area for placing the I/O pad cells, core area with spacing the I/O pads, rows or columns or both in the core area. The designer may also create a power grid prior to placement. This step may also include placement of cell groups or macro blocks to optimize the connectivity be- tween groups and blocks. The automatic placement tests potential placements for the design and tries to optimize the placement for overlap removal, routing congestion balancing, power balancing, wire length and timing assurance.

Extraction and Delay Calculation: This step is needed to extract parasitic capacitance and resistance from the layout to calculate and apply delays in static timing analysis and/or full timing simulation using System Verilog. The parasitic information is extracted from the layout, and interconnects delays included in the SPF (Standard Parasitic Format) file. -

Pre-Clock Tree Synthesis Timing Check: T h e static timing analysis should be performed using projected parasitics to verify that all timing goals/constraints set after synthesis are still met.

Clock Tree Generation: The designer has to build a clock tree when a large number of cells are clocked by a single driver cell. In this case we are trying to control the signal skew at the clocked cell's input. It is assumed that the physical library includes timing data in a Timing Library Format (TLF). All modifications to the net list are saved in a DEF (Design Exchange Format) file for back annotation to the original net list.

Routing: This step includes global and final routing. Global routing usually consists of a coarse regular wiring layout based on obstructions resulting from special wiring, clock wiring and placement. Analyzing the routing congestion map before at- tempting the final routing is recommended. Final routing creates the detailed regular wiring layout. Post layout timing analysis may be done after routing. It can be done by back annotation of SDF file.

Post Layout Static Timing Analysis : Using SDF, CAP and RES files with accurate timing information post layout simulation and timing verification can be performed by back annotating the SDF file.

DRC & LVS verification: It is very important to run DRC and LVS on the layout to be sure that the connectivity, the geometry and the spacing are correct and the layout matches the schematic. This step includes a flat extraction of the layout.

Block Specification Update: After each block is done, it is possible that an update on the block specs is required and therefore the respective block documentation will have to be modified. To verify the updated behavioral model and physical layout of each block, the designer needs to perform two simulations from the top level, one with and one without circuit instantiation of the target block. Other blocks should remain at the behavioral or RTL level for these simulations. The same test bench created at the partitioning and behavioral modeling stage should be used for this regression simulation.

3.4 Top Level Layout Design.

At this stage of the flow, the layout of all analog and digital blocks is ready and we have to integrate them. Cadence Aligrow 15.2 can be used to perform schematic driven placement for the blocks at the top level based on the top level schematic created earlier at the partitioning stage. DRC and LVS are per- formed to ensure correctness of the layout. Figure 2.5 shows this part of the design flow. Post layout extraction and

simulation are done to verify the top level parasitic modeling. Any errors revealed by DRC/LVS or any undesirable parasitics revealed by post layout simulation need to be corrected by going back to top level layout or block layout

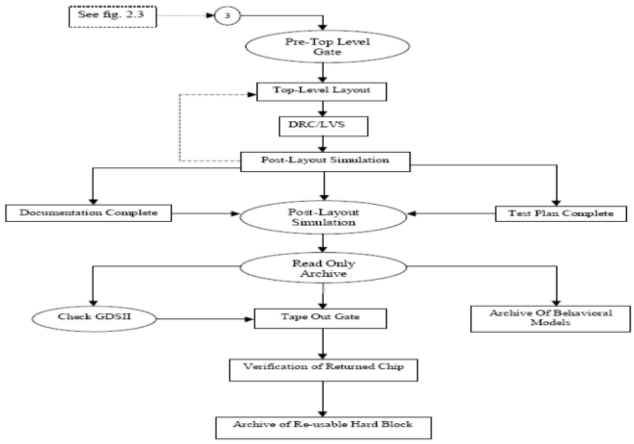

Figure 2.5 Chip integration

Post Layout Gate: When the top level design passes post layout simulation, a post layout gating should be done. Gating is a peer review of the process to ensure that a post layout simulation has been performed properly and to check on manufacturing issues such as power/thermal considerations, metal migration issues, power IO to signal IO ratio, ground bounce problem, proper design ID.

Complete Documentation & Test Plan: In parallel, top level design documentation needs to be completed or updated after successful post layout simulation and so does the test plan. At this point, the exact test setup or procedures down to what pin is connected to what instrumentation through what fixturing can be described. All that will converge back to post layout gating. Complete design documentation and test plan are essential components of passing the post layout gate.

Read Only Archive: After passing the post layout gate, a read only library (ROL) should be created to archive the de- sign. Preferably the design data is archived in a standard data formats such as GDSII/DEF/LEF. The design must be frozen at this point so the right version of the design can be used for debugging later on. Archiving designs using consistent format, style, directory structures makes re-use easier. For re-use purposes, it is even more important to archive the technology independent behavioral models than the physical data files. The behavioral models must be properly documented and stored. Before sending out the GDSII file for fabrication, it is desirable to read the file back into Cadence to perform an LVS against the original layout to ensure there are no translation problems occurred.

Tape Out: The GDSII file can then be sent out for fabrication.

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